



5-STAGE JOHNSON COUNTER

The HEF4017B is a 5-stage Johnson decade counter with ten spike-free decoded active HIGH outputs (O_0 to O_9), an active LOW output from the most significant flip-flop (\bar{O}_{5-9}), active HIGH and active LOW clock inputs (CP_0, \bar{CP}_1) and an overriding asynchronous master reset input (MR).

The counter is advanced by either a LOW to HIGH transition at CP_0 while \bar{CP}_1 is LOW or a HIGH to LOW transition at \bar{CP}_1 while CP_0 is HIGH (see also function table).

When cascading counters, the \bar{O}_{5-9} output, which is LOW while the counter is in states 5, 6, 7, 8 and 9, can be used to drive the CP_0 input of the next counter.

A HIGH on MR resets the counter to zero ($O_0 = \bar{O}_{5-9} = \text{HIGH}$; O_1 to $O_9 = \text{LOW}$) independent of the clock inputs (CP_0, \bar{CP}_1).

Automatic code correction of the counter is provided by an internal circuit: following any illegal code the counter returns to a proper counting mode within 11 clock pulses.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

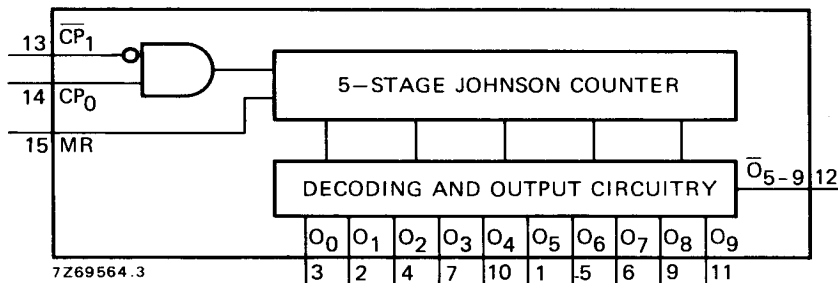


Fig. 1 Functional diagram.

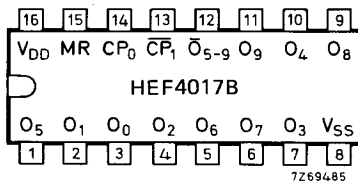


Fig. 2 Pinning diagram.

HEF4017BP : 16-lead DIL; plastic (SOT-38Z).
HEF4017BD : 16-lead DIL; ceramic (cerdip) (SOT-74).
HEF4017BT : 16-lead mini-pack; plastic (SO-16; SOT-109A).

PINNING

CP_0 clock input (LOW to HIGH triggered)
 \bar{CP}_1 clock input (HIGH to LOW triggered)
MR master reset input
 O_0 to O_9 decoded outputs
 \bar{O}_{5-9} carry output (active LOW)

FAMILY DATA

I_{DD} LIMITS category MSI

} see Family Specifications

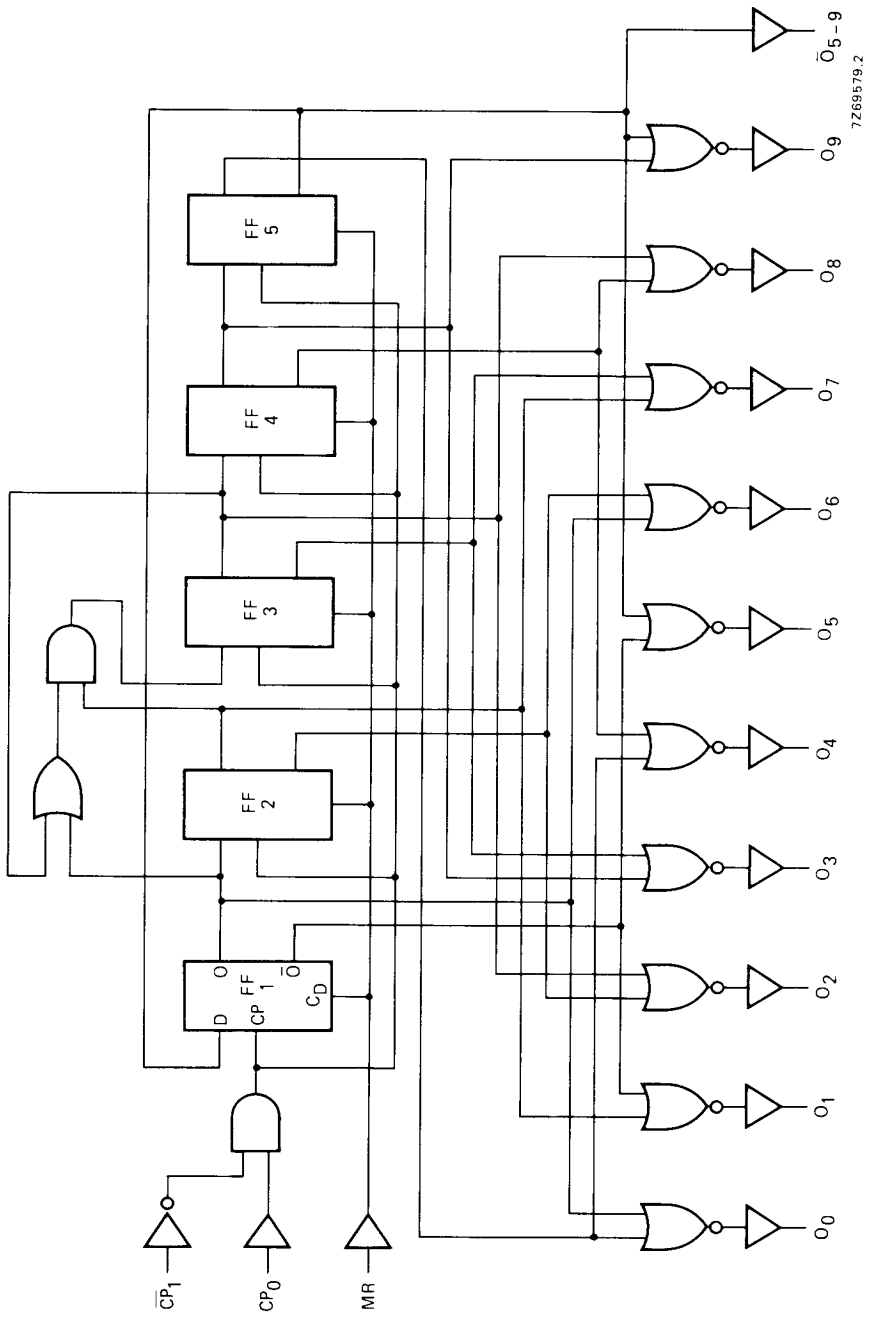


Fig. 3 Logic diagram.

FUNCTION TABLE

MR	CP ₀	\overline{CP}_1	operation
H	X	X	O ₀ = \overline{O}_{5-9} = H; O ₁ to O ₉ = L
L	H	\searrow	Counter advances
L	\swarrow	L	Counter advances
L	L	X	No change
L	X	H	No change
L	H	\swarrow	No change
L	\searrow	L	No change

H = HIGH state (the more positive voltage)

L = LOW state (the less positive voltage)

X = state is immaterial

 \swarrow = positive-going transition \searrow = negative-going transition

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	symbol	min.	typ.	max.	typical extrapolation formula
Propagation delays						
CP ₀ , \overline{CP}_1 → O ₀ to O ₉ HIGH to LOW	5	t _{PHL}	140	280	ns	113 ns + (0,55 ns/pF) C _L
	10		55	110	ns	44 ns + (0,23 ns/pF) C _L
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	125	250	ns	98 ns + (0,55 ns/pF) C _L
	10		50	100	ns	39 ns + (0,23 ns/pF) C _L
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L
CP ₀ , \overline{CP}_1 → \overline{O}_{5-9} HIGH to LOW	5	t _{PHL}	145	290	ns	118 ns + (0,55 ns/pF) C _L
	10		55	110	ns	44 ns + (0,23 ns/pF) C _L
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L
LOW to HIGH	5	t _{PLH}	125	250	ns	98 ns + (0,55 ns/pF) C _L
	10		50	100	ns	39 ns + (0,23 ns/pF) C _L
	15		40	80	ns	32 ns + (0,16 ns/pF) C _L
MR → O ₁ to O ₉ HIGH to LOW	5	t _{PHL}	115	230	ns	88 ns + (0,55 ns/pF) C _L
	10		50	100	ns	39 ns + (0,23 ns/pF) C _L
	15		35	70	ns	27 ns + (0,16 ns/pF) C _L
MR → \overline{O}_{5-9} LOW to HIGH	5	t _{PLH}	110	220	ns	83 ns + (0,55 ns/pF) C _L
	10		45	90	ns	34 ns + (0,23 ns/pF) C _L
	15		35	70	ns	27 ns + (0,16 ns/pF) C _L
MR → O ₀ LOW to HIGH	5	t _{PLH}	130	260	ns	103 ns + (0,55 ns/pF) C _L
	10		55	105	ns	44 ns + (0,23 ns/pF) C _L
	15		40	75	ns	32 ns + (0,16 ns/pF) C _L
Output transition times						
HIGH to LOW	5	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L
LOW to HIGH	5	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
	10		30	60	ns	9 ns + (0,42 ns/pF) C _L
	15		20	40	ns	6 ns + (0,28 ns/pF) C _L

A.C. CHARACTERISTICS

$V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	
Hold times $CP_0 \rightarrow \overline{CP_1}$	5	t_{hold}	90	45	ns	see also waveforms Figs 4 and 5
	10		40	20	ns	
	15		20	10	ns	
$\overline{CP_1} \rightarrow CP_0$	5	t_{hold}	80	40	ns	
	10		40	20	ns	
	15		30	10	ns	
Minimum clock pulse width: $CP_0 = \text{LOW}$; $\overline{CP_1} = \text{HIGH}$	5	$t_{WCPL} =$	80	40	ns	
	10		40	20	ns	
	15	t_{WCPH}	30	15	ns	
Minimum MR pulse width; HIGH	5	t_{WMRH}	50	25	ns	
	10		30	15	ns	
	15		20	10	ns	
Recovery time for MR	5	t_{RMR}	60	30	ns	
	10		30	15	ns	
	15		20	10	ns	
Maximum clock pulse frequency	5	f_{max}	6	12	MHz	
	10		12	24	MHz	
	15		15	30	MHz	

	V_{DD} V	typical formula for P (μW)	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load cap. (pF) $\Sigma(f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$500 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$2200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$6000 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

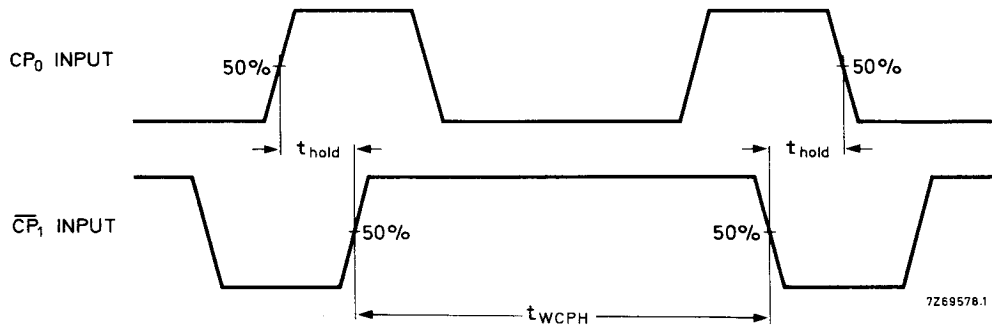


Fig. 4 Waveforms showing hold times for CP_0 to \overline{CP}_1 and \overline{CP}_1 to CP_0 . Hold times are shown as positive values, but may be specified as negative values.

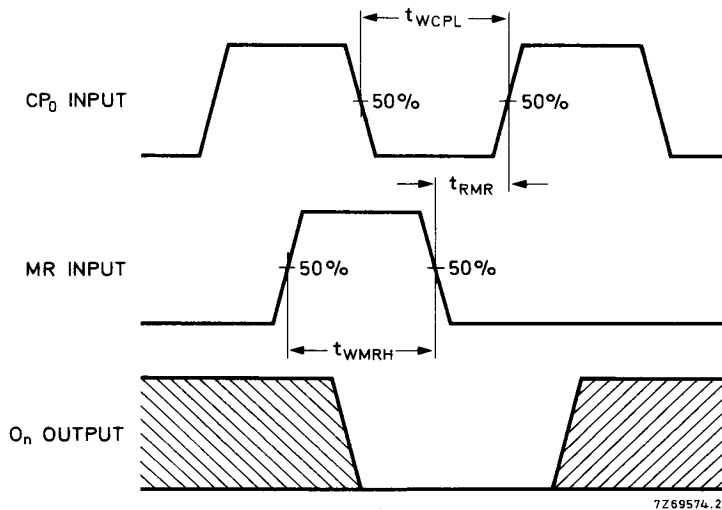


Fig. 5 Waveforms showing recovery time for MR; minimum CP_0 and MR pulse widths. Conditions: $\overline{CP}_1 = \text{LOW}$ while CP_0 is triggered on a LOW to HIGH transition. t_{WCP} and t_{RMR} also apply when $CP_0 = \text{HIGH}$ and \overline{CP}_1 is triggered on a HIGH to LOW transition.

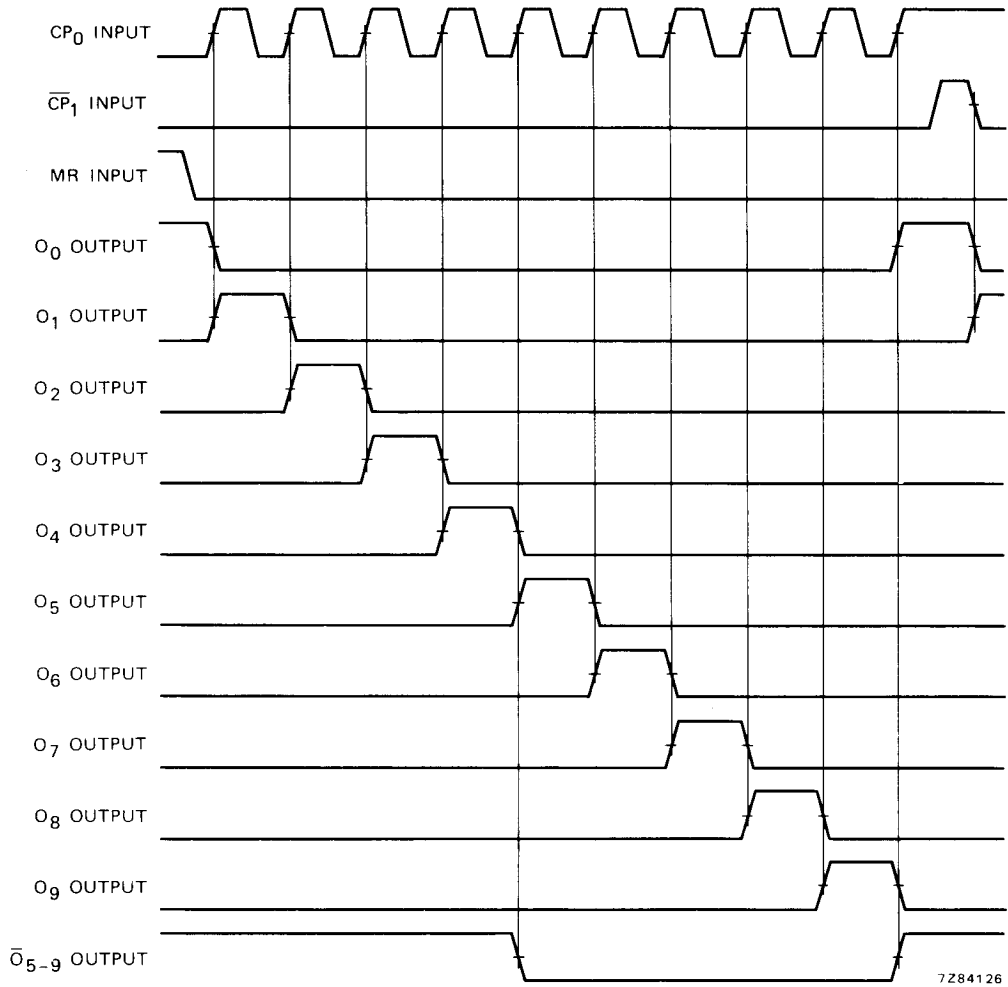


Fig. 6 Timing diagram.

APPLICATION INFORMATION

Some examples of applications for the HEF4017B are:

- Decade counter with decimal decoding
- 1 out of n decoding counter (when cascaded)
- Sequential controller
- Timer.

Figure 7 shows a technique for extending the number of decoded output states for the HEF4017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

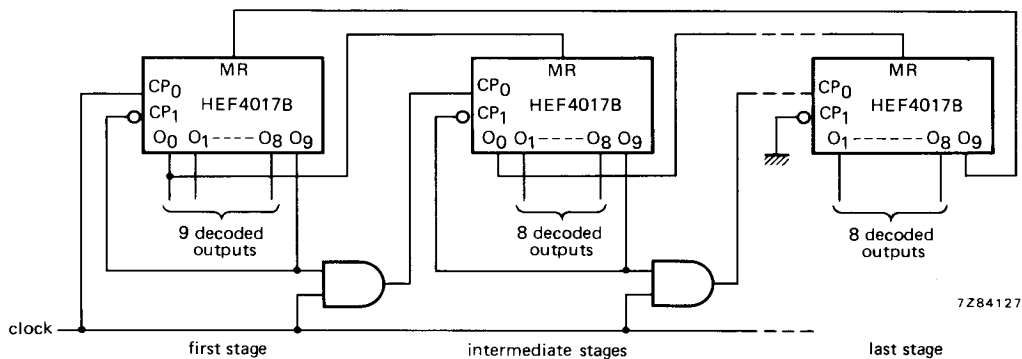


Fig. 7 Counter expansion.

Note

It is essential not to enable the counter on \overline{CP}_1 when CP₀ is HIGH, or on CP₀ when \overline{CP}_1 is LOW, as the this would cause an extra count.